Hybrid Postprocessing Etching for CMOS-Compatible MEMS

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***Abstract*— A major limitation in the fabrication of microstructures as a postCMOS (complimentary metal oxide semiconductor) process has been overcome by the development of a hybrid processing technique, which combines both an isotropic and anisotropic etch step. Using this hybrid technique, microelectromechanical structures with sizes ranging from 0.05 to ~1 mm in width and up to 6 mm in length were fabricated in CMOS technology. The mechanical robustness of the microstructures determines the limit on their dimensions. Examples of an application of this hybrid technique to produce microwave coplanar transmission lines are presented. The performance of the micromachined microwave coplanar waveguides meets the design specifications of low loss, high phase velocity, and 50-Ω characteristic impedance. Various commonly used etchants were investigated for topside maskless postmicromachining of ⟨100⟩ silicon wafers to obtain the microstructures. The isotropic etchant used is gas-phase xenon difluoride (XeF_2), while the wet anisotropic etchants are either ethylenediamine-pyrocatechol (EDP) or tetramethylammonium hydroxide (TMAH). The advantages and disadvantages of these etchants with respect to selectivity, reproducibility, handling, and process compatibility are also described. [258]**

***Index Terms*— CMOS microwave elements, isotropic and anisotropic silicon etching, maskless etching, microelectromechanical systems (MEMS), micromachining, suspended transmission lines.**

I. Introduction

In RECENT years, there has been growing interest in the research and development of integrated microelectromechanical systems (MEMS). Various pressure sensors, accelerometers [1], and millimeter-wave components [2], [3] have been fabricated using specialized processes with backside micromachining. Specialized processes may not automatically allow for on-chip integration of electronics and require the development and implementation of a circuit process along with the MEMS process. Backside etching also involves additional masks and alignment and therefore adds more complexity. Concurrently, there is also strong interest in developing microtransducers that are compatible with a commercial complimentary metal-oxide semiconductor (CMOS) process. In this paper, we have chosen to focus on microtransducers, which can be implemented in a commercial CMOS foundry technology. Precursors for the microtransducers integrated with the necessary electronics are fabricated through a commercial CMOS foundry, available through the MOSIS[1] service. Compatibility with a commercial CMOS process allows for monolithic integration of analog and digital circuits, which provide signal conditioning, interface control, and wireless remote communication. After receiving the precursor chips from the foundry, the microsensors or microactuators are then released by an additional maskless frontside postprocessing etch. Examples of these CMOS-compatible microsystems are temperature sensors [4], flow sensors [5], infrared thermal displays [6], microwave components [7], [8], and solid-state conductometric chemical gas sensors [9].

Silicon micromachining is the key technology to fabricate microtransducers and actuators. To realize microtransducers at low cost, there are several requirements on the postprocessing etching. The chemical etchants must be compatible with materials used in the commercial CMOS processes, namely, silicon dioxide, silicon nitride, and exposed aluminum. The etchants must not contaminate the gate dielectrics with impurities such as mobile alkali ions, which shift the flatband voltage and affect the circuits otherwise. Commonly used anisotropic etchants are ethylenediamine-pyrocatechol (EDP), tetramethylammonium hydroxide (TMAH), and ammonium hydroxide. More recently, xenon difluoride (XeF_2) has become a popular isotropic etch for micromachining. Depending on the design, the suspended microtransducers can be realized using either an isotropic or anisotropic etch. Finally, other requirements for these etchants are ease of handling and safety.

While the above-mentioned CMOS-compatible microtransducers with size ranging from 40–200 μm can readily be realized with either an isotropic or anisotropic postetching, larger or longer microstructures, such as microwave coplanar waveguides and passive components, cannot be achieved with

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[1]Certain commercial products are identified in this paper to specify the procedure adequately. This does not imply recommendation or endorsement by NIST nor does it imply that those commercial products are the best available for the purpose.

either an isotropic or anisotropic etch alone. Large structures require unacceptably long anisotropic etch times, which, in turn, cause other negative effects. When the waveguides are fully suspended, the aggressive EDP etchant attacks the glass layers and etches away the exposed aluminum on the bonding pads, making the device mechanically unstable. Therefore, etching is the limiting factor in realizing large suspended microstructures.

In this paper, we present a novel micromachining methodology, which combines an isotropic etch step and an anisotropic etch step to release large or long suspended microstructures. Length independent microstructures can be achieved with clever design. Also, using our methodology, design placement of dielectric openings, which expose the substrate to the etchant, is significantly simpler and allows much more flexibility in the layout. This, in turn, results in significantly improved mechanical robustness since larger areas of supporting glass remain.

Detailed characteristics of the isotropic etchant are presented in Section II and those of the anisotropic etchants in Section III. In Section IV, we discuss the novel hybrid technique and give an example of the fabrication of long microwave coplanar waveguides.

II. Xenon Difluoride (XeF_2) Etching of Silicon

The use of XeF_2 for plasma etching of silicon and etching silicon with XeF_2 without plasma has been studied extensively for the last 15 years. Silicon is isotropically etched by exposure to gaseous XeF_2 at room temperature. Only recently has XeF_2 without plasma enhancement been used to micromachine silicon to create microtransducers. Chung *et al.* [9], [10] have performed a detailed study of the etching characteristics of XeF_2. An investigation of the mechanisms of the etching of silicon with vapor XeF_2 was given by Houle [11] and Winters and Coburn [12]. Hence, this section only gives a brief description of the proposed etching mechanisms. Rather, the etching characteristics and practical applications of XeF_2 to realize microtransducers are described in detail.

XeF_2 is a white crystalline solid with a vapor pressure of about 600 Pa (4.5 Torr) at room temperature [11]. The reaction between XeF_2 and silicon occurs through a sequence of steps. Gaseous XeF_2 is first absorbed on the silicon and then reacts to form a thick layer of fluorosilyl consisting of SiF, SiF_3, and SiF_4. The fluorosilyl product desorbs into the gas phase. The principal gas-phase product has been determined to be SiF_4, which is volatile at room temperature. The reaction equation for XeF_2 and silicon is approximately given by

$$2XeF_2 + Si \rightarrow 2Xe + SiF_4. \quad (1)$$

It is relatively easy and inexpensive to set up the apparatus for XeF_2 etching because XeF_2 sublimes at a pressure of $\sim$600 Pa (4.5 Torr) at 300 K. The system used at NIST consists of a short stainless-steel T-section vacuum chamber connected to a mechanical vacuum pump with a liquid nitrogen cold trap, pressure gauge, nitrogen gas inlet, XeF_2 source compartment, and sample interchange with electrical feedthroughs. The system can also be equipped with an optical microscope, which provides visual monitoring of the etching process through an optical window. XeF_2 vapor is introduced into the vacuum chamber by opening and closing a valve, which provides isolation of the solid XeF_2 from the vacuum. Since XeF_2 reacts with moisture to form highly corrosive hydrofluoric acid, the XeF_2 source should be kept in a dry box. The entire system is located in a fumehood, and the etching process is fully automated. All valves are controlled by a computer through a data-aquisition and signal-generating interface.

A XeF_2 etch is performed in short cycles of 30-s duration, consisting of the following. The vacuum chamber is first pumped down to 2.7 Pa (20 mTorr) before opening the XeF_2 valve. After closing the vacuum valve, XeF_2 flows into the chamber until a target pressure of 400 Pa (3.0 Torr) is reached. This may take up to about 10 s, at which point the XeF_2 valve is closed and a waiting time of about 20 s is allowed for etching. Silicon does not start etching instantaneously upon exposure to XeF_2: it first requires the formation of a few fluorosilyl layers. The chamber is then backfilled with nitrogen gas and the dominant volatile byproduct SiF_4 is pumped from the chamber until its pressure is below 2.7 Pa (20 mTorr) before the next cycle begins. In this method, which is called the pulse method, the actual etch rate of silicon varies depending on the amount of exposed silicon and other parameters such as temperature. The effect of silicon loading and temperature dependence has been examined by Chung [10].

XeF_2 is fully compatible with materials used in commercial CMOS processes. Namely, no noticeable attack of silicon dioxide, silicon nitride, and aluminum is found. Consequently, a thin layer of silicon dioxide can be used as a mask for the etching of silicon. XeF_2 is extremely selective to silicon and, thus, is perhaps an ideal postCMOS etchant. However, in this work XeF_2 was found to attack iridium and gold. About 30 nm of gold was etched away after ten pulses of XeF_2 etch. This contradicts the finding of Chung [10] who reported that XeF_2 does not attack gold. Also, a commercial vacuum gauge with a gold-plated sensor, which was connected to the XeF_2 etching chamber, became nonfunctional after exposure to several pulses of XeF_2 gas. It is unusual to find that XeF_2 attacks both gold and iridium since they are relatively inert materials. The attack of Ir is shown in the scanning electron microscope (SEM) picture in Fig. 1. Pinholes on Ir created after about 15 pulses of XeF_2 etch are clearly visible. We have also observed XeF_2 attack on tungsten and silver films, but have not yet quantified the effects.

Etching with XeF_2 is applicable to packaged as well as unpackaged chips. For unpackaged chips, photoresist can be used to protect the backside and peripheries of the chip because XeF_2 will etch any exposed silicon, resulting in significant thinning of the chip. The glass openings (*open* areas in Magic CAD), defined by the superposition of an active area, active-contact cut, via cut, and glass cut in the layout file, are areas where the silicon surface is exposed for etching. If the glass openings are fabricated from the foundry according to

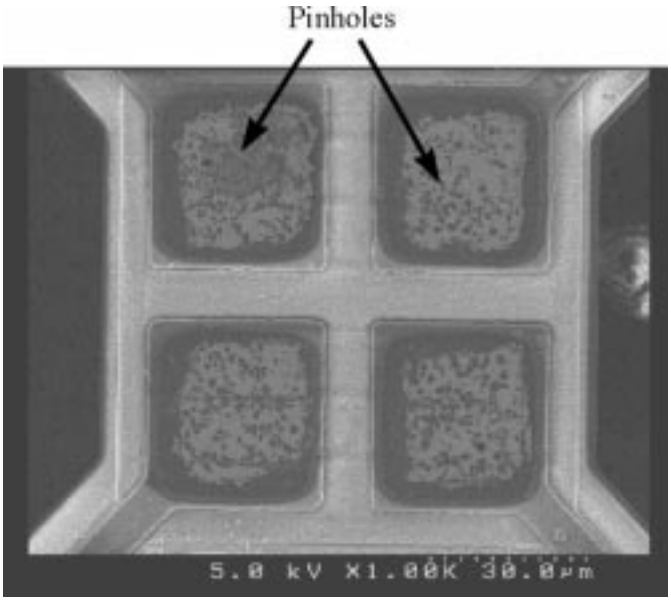


Fig. 1. SEM picture showing pinholes in iridium attacked by XeF_2 after about 15 pulses of etching.

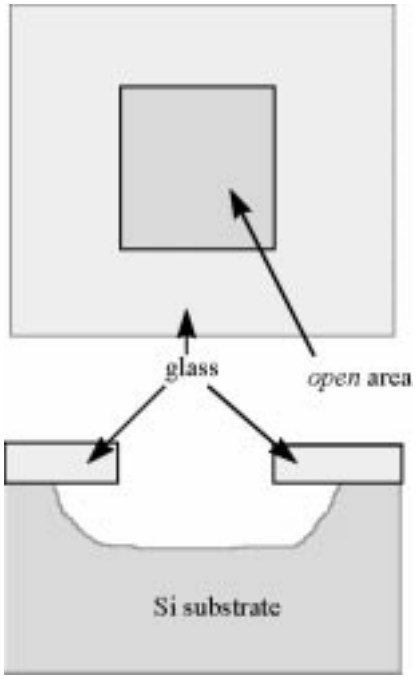


Fig. 2. Top view and a cross section of isotropic etching of silicon by gaseous XeF_2 using SiO_2 as the mask.

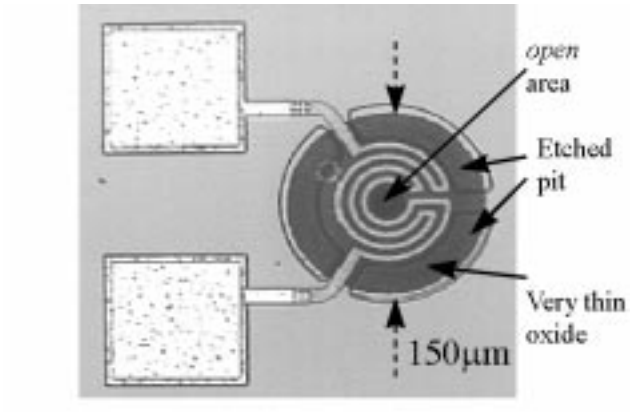
the design specifications, the silicon surface in those areas is covered only with a very thin layer of native oxide. In most cases, no stripping of the native oxide layer is necessary, and the chips are readily etched. In some cases, however, due to process modifications at the foundry, sufficient glass remains in the openings to prevent etching. To assure etching of the desired areas, it is recommended that the thin layer of native oxide be removed by a 10-s dip in buffered hydrofluoric acid (HF) before etching. Also, since moisture reacts with XeF_2 to form hydrofluoric acid, which attacks SiO_2, the chips are baked at 120 °C prior to etching.

Microtransducers that are designed for XeF_2 etching should reflect the isotropy of the etching profile. Because of the high silicon selectivity of XeF_2 in CMOS processes, SiO_2 may be used as the mask. The isotropic etching creates small cavities around each glass opening, which propagate radially outward, resulting in an etched pit shaped like a bathtub as shown in Fig. 2. Shown in Fig. 3(a) is an example of a new microheater design, which takes advantage of the isotropy of the XeF_2 etch. A small 20-μm-diameter glass opening exposes the silicon for etching. The etching undercuts the microstructure, which is 80 μm in diameter, and suspends it. For better thermal isolation, only a thin layer of SiO_2 about the thickness of the gate oxide is left suspended between the microheater and substrate. This is incorporated into the design with the glass cut, via cut, and active layer in the layout file.

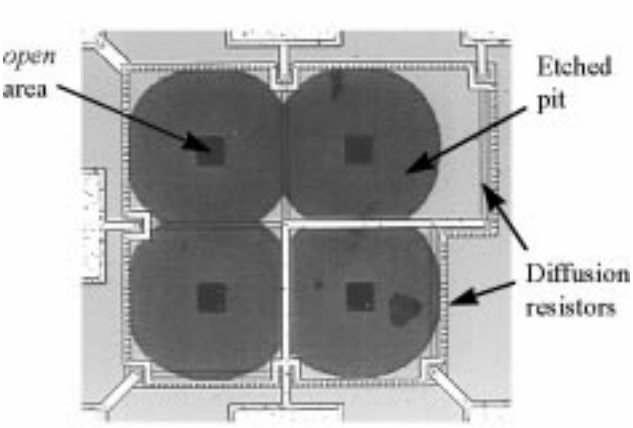
XeF_2 etches silicon very rapidly, making dimensional control very difficult. To determine when the etch process is complete, an on-chip test structure can be monitored. An example of a test structure for monitoring the microheaters and coplanar microwave transmission lines is shown in Fig. 3(b). Two quadrants are designed with parallel n-diffusion resistors, which are electrically monitored. When XeF_2 etches away the first n-diffusion resistors in either the vertical or horizontal directions, about 5 μm more etching is needed. At this point, the pulse duration is reduced to provide better control. Since the etch rate of silicon is more linear at pressures over the range 10^{-6} Pa (10^{-8} Torr)–66.6 Pa (0.5 Torr), another way to terminate the etching with high precision is to etch at a lower pressure. In either case, when an open circuit is detected in the second n-diffusion resistor, etching is terminated. This test structure allows for submicrometer-precision control of XeF_2 etching. For most micromachined transducers, this level of control is sufficient. An advantage of employing gas-phase XeF_2 over liquid anisotropic etchants like EDP or TMAH is improved reliability giving yields close to 100%. In wet anisotropic etching, thin membranes cannot be fabricated due to hydrogen bubbles adhering to the surface. These problems do not occur in gas-phase etching using XeF_2, and gate oxides ($\sim$40 nm thick) have successfully been used as membranes to suspend structures as far as 25 μm from the edge of the etch pit, as shown in Fig. 3.

III. Anisotropic Wet Etching of Single-Crystal Silicon

In anisotropic etching, silicon is selectively removed at a rate which depends on the orientation of the crystal lattice structure. In general, the etch rate of $\{100\}$ crystal planes is more than twenty times faster than the etch rate of the $\{111\}$ planes for most anisotropic etchants. Silicon substrates used in CMOS processes are (100) oriented, and an inverted truncated pyramid-type pit is formed by anisotropic etching as shown in Fig. 4. The side walls of the pit are bounded by the $\{111\}$ planes, which make a 54.7° angle with the substrate surface. In standard CMOS foundries, the wafers are supplied with a flat parallel to the $\{110\}$ planes, which is used for alignment. The design considerations to achieve suspended microtransducers with frontside maskless postprocessing etching have



(a)



(b)

Fig. 3 (a) Microheater designed for XeF_2 etching. (b) Test structure for monitoring microheater and microwave coplanar waveguide in XeF_2 etching. Pad size is 100 μm $\times$ 100 μm.

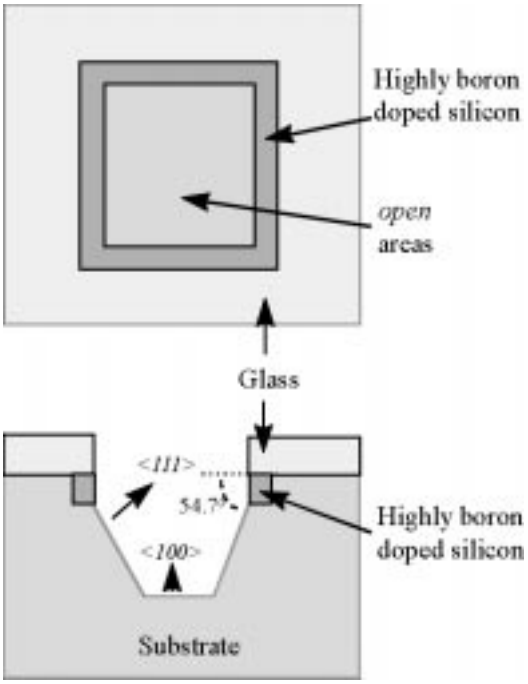


Fig. 4. Top view and cross section of etched pit bounded by ⟨111⟩ planes fabricated by anisotropic etching using highly boron-doped silicon as the etched stop.

already been reported extensively [13] and are not discussed here.

Commonly used wet anisotropic etchants can be classified into three types: 1) alkali metal hydroxides [14]; 2) diamines-based [15]; and 3) quaternary ammonium hydroxides [16]–[19]. Alkali metal hydroxides such as potassium hydroxide (KOH) have a high silicon etch rate and anisotropy. Unfortunately, KOH is not postCMOS compatible because it attacks aluminum and SiO_2 and contaminates the gate oxides with mobile alkali metal ions. EDP is a commonly used etchant and is discussed in Section III-A. The quaternary ammonium hydroxides fulfill the requirements of CMOS compatibility and are still being investigated for micromachining applications. In this group, tetramethylammonium hydroxide (TMAH) is the preferred etchant because it has a fairly high silicon etch rate. However, despite many reports in the literature [16]–[19], it is still not well understood, and reproducibility is still a big problem. In Section III-B, our current experience with the properties of TMAH is described. Another CMOS etchant, which might be a potential candidate for silicon micromachining, is ammonium hydroxide doped with dissolved silicate and hydrogen peroxide [20]. Aqueous ammonium hydroxide was not considered here because it has a very low silicon etch rate, poor reproducibility, and problems with hillock formation. The parameter window for ammonium hydroxide to work properly is very small, hence, a high-accuracy real-time monitoring of the loss of ammonia, OH^- ion, hydrogen peroxide, and contaminants appeared to be needed. Only small chips have been etched successfully with this etchant in this work; larger chips and chips that were packaged did not even start to etch.

The apparatus for anisotropic etching is very simple. The entire system, which consists of a hotplate, magnetic stirring bead, pyrex glass beaker, thermometer, nitrogen gas bubbler, and reflux condenser to minimize the loss of water is placed inside the fumehood.

A. Ethylenediamine-Pyrocatechol Water

EDP water with a small amount of pyrazine is a well-established etchant for the anisotropic etching of single-crystal silicon and finds extensive application in silicon micromachining [14], [15]. There are several types of EDP etchants with different compositions, known as types B, T, S, and F. Types T and F have a high silicon etch rate while types B and S have a low silicon etch rate. They are readily commercially available. Only types S and F are used in this work. Type F has a higher water and pyrocatechol content than type S. We used type F almost exclusively because type S attacked exposed aluminum (e.g., bonding pads) more vigorously during the longer etch time required for type S to fully release the structures. This finding contradicts results of Lenggenhager [21], who reported that type S is the preferred anisotropic etchant for CMOS-compatible microtransducers because it has the highest selectivity between silicon and

aluminum. This apparent contradiction may be caused by the differences between the chip-fabrication processes at the respective foundries used.

Fresh EDP-type-F etchant has a pale amber color, which darkens after a few hours of use and exhibits a deep red color when it becomes unusable. Etching is generally performed in the temperature range 92°–100 °C, which gives an etch rate of about 70 μm/h for (100) silicon. The etch rate increases as the solution is exposed to air for some time. EDP etching is a relatively awkward process, and chips etched with EDP tend to deteriorate over a long period of time unless they are rinsed very well for many hours after etching. The problem with EDP, when used at lower temperatures, is the formation of a thin layer of insoluble residue. If this residue is not washed away, it will destroy all the structures on the chip by corrosion. The cleaning procedure starts with rinsing in a low flow rate of deionized (DI) water for 20 min. The chips are then left in a large bath of DI water for 8–12 h. Significantly shorter time in the DI water bath does not remove all of the adsorbed EDP from the chip and/or package, resulting in long-term residue buildup and undesired further etching. Care must be taken to avoid damaging the suspended microstructures during cleaning. No visible residue was observed for type F when etched in the above temperature range. An SEM picture of a CMOS-compatible microhotplate designed to detect gases is shown in Fig. 5(a), and a customized version of this chip with tungsten contacts is shown in Fig. 5(b). Unlike the quaternary ammonium hydroxide etchants, EDP has no problem with the formation of "hillocks," which tend to stop the etching prematurely. The etched surfaces of (100) (bottom of the etched pit) and (111)-oriented (side walls of the etched pit) silicon are quite smooth as shown in Fig. 5(b). One main advantage of using EDP is that etching is self-terminated by highly boron-doped silicon, which is a very effective etch stop. EDP-type F is only moderately selective against aluminum (*metal1* and *metal2* in the MOSIS 2-μm process) and will etch away all the aluminum on the bonding pads in 2 h, therefore, this must be taken into consideration when designing microtransducers for EDP etching.

The use of EDP is not as desirable as the quaternary ammonium hydroxide etchants because it is considered quite hazardous. EDP can have very serious long-term toxic effects and can be absorbed through the skin. When it comes in contact with water during cleaning, a visible amber mist develops. Misting creates a serious inhalation hazard in addition to that caused by the evaporation of ethylenediamine from solution. Care must be taken not to breathe any of these vapors during the etching process.

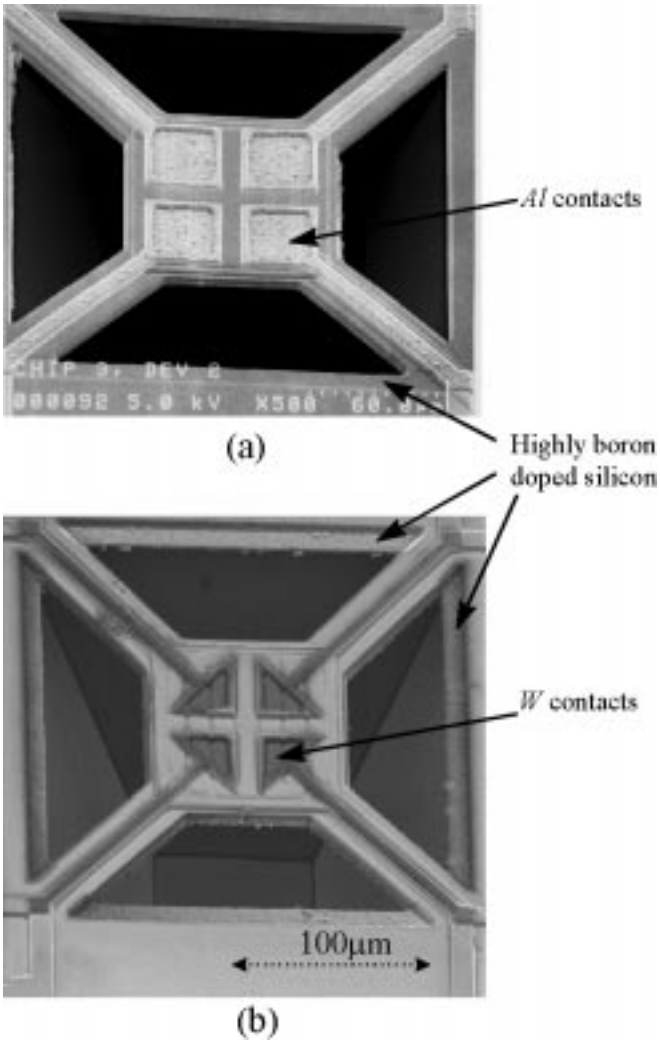


Fig. 5. Microhotplate conductometric chemical gas sensors etched in EDP from (a) a CMOS process. (b) A specialized process with tungsten contacts.

B. Tetramethylammonium Hydroxide

A mixture of tetramethylammonium hydroxide (TMAH), water, silicic acid (SA), and ammonium peroxydisulfate (APODS) is another selective anisotropic etchant for silicon that has been described recently [18]. The SA increases the selectivity against aluminum through the formation of aluminosilicates, which are less soluble in solutions with a moderate pH. The APODS prevents the formation of hillocks on etching surfaces in TMAH solutions with pH lower than about 13. When hillocks cover a substantial fraction of the surface of an etch pit, the etch rate is substantially reduced [17]–[19]. This etchant is much less hazardous to work with than EDP because it is not very volatile and does not mist. When TMAH is heated to 130 °C, it decomposes into methanol and trimethylamine. Apparently, decomposition also occurs during etching since the characteristic rotten-fish odor of trimethylamine is noticeable in solutions that have been used for a few hours.

The recipe used in the present work was as follows. In a graduated beaker, about 600 mL of DI water was mixed with 600 mL $\pm$ 30 mL of 25% wt. TMAH, and the contents poured into a 1-L bottle containing 100 g of 100-mesh SA (95% $\pm$ 5% SiO_2) as obtained from the manufacturer of the SA. The reason for this mixing procedure was to minimize airborne SA particles. The resulting mixture was then shaken vigorously and poured into a larger container to which was added enough DI water to bring the volume to between 2200–2300 mL. The solution prepared in this way corresponds to about 7%

TABLE I
TMAH PREPARATION PROCEDURE

Step	Procedure
1	Add 600 mL deionized water with 600 mL of 25% tetramethylammonium hydroxide solution.
2	Pour contents into a bottle containing 95 g ± 5 g of 100 mesh silicic acid (SA), and shake the mixture well.
3	Pour the mixture into a bigger container, add 1000 mL deionized water, and shake well.
4	Pour mixture into a beaker with a reflux condenser, and heat to 80 °C under high stirring.
5	If the mixture is clear, add 5 g of ammonium peroxydisulfate (APODS); otherwise, discard the mixture.
6	If the mixture becomes clear, reduce stirring to the appropriate value and place the chips to be etched in the beaker.
7	Remove the chips after 30 to 40 min, add 8 mL 25% TMAH followed by 5 g APODS to the etching solution, and replace the chips in the beaker if the solution becomes clear within 10 min.
8	Repeat step 7 as many times as necessary to complete the etch.

TMAH ion concentration with a much lower hydroxide ion concentration due to neutralization by SA. The passivation of aluminum required about 40-g/L SA for this concentration of TMAH [18].

When prepared as described above, the resulting mixture of reagents was very cloudy, almost milky, which shows that at least some of the SA was present as a suspension rather than as dissolved silicate. If the mixture became clear after heating to 80 °C, 5 g/L of APODS was added while the solution was stirred vigorously. On the other hand, if either the original mixture or the mixture containing APODS did not become clear or almost clear after 10 min of rapid stirring at 80 °C, it was discarded.

Chips to be etched were put into the clear TMAH etchant solution at 80 °C with moderate stirring and removed after 30 or 40 min. By this time, the etch rate had decreased significantly due to decomposition of the APODS, which is catalyzed by high pH. After the chips were removed, about 16-mL 25% TMAH and 5-g APODS per liter were added to the mixture in that order while the solution was stirred vigorously. If the mixture cleared significantly within 10 min, then the chips were returned to the solution for another 30–40 min of etching. Otherwise, the mixture was discarded, and the etch continued with new etchant. Usually, the etch was complete after two exposures to the etchant for 30–40 min, but occasionally a third exposure of the same duration was needed. This procedure is summarized in Table I.

The TMAH solution prepared by the procedure described above was used to etch thermal pixel array (TPA) chips containing 64-by-64 pixel arrays of microheating systems.

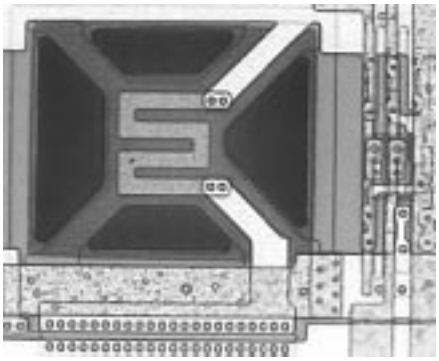


Fig. 6. A microheater element etched in TMAH solution.

Each pixel consisted of a digital address circuit, analog drive circuit, and microheater suspended over an etch pit as shown in Fig. 6. Twenty TPA chips were etched following the above procedure, and at least 15 of these were clearly etched well enough for subsequent testing. This meant that all of the heaters were fully released with a clearance of at least 30 μm to the bottom of etch pits of approximately uniform depth and that all of the aluminum bonding pads were intact.

The results of this etching procedure were fairly reproducible. By contrast, the procedure described in [18] was completely irreproducible in our hands, probably due to our failure to follow the procedure properly. Localized deposits of silica gel, which decreased the etch rate under the deposit, were a major problem. Other problems included frequent premature termination of the etch with hillock formation and

occasional failures of the etchant to even start removing silicon. Besides the 20 TPA chips mentioned above, TPA chips that were not fully etched with the procedure of [18] were successfully completed with our procedure described above.

Despite a reasonable level of success with this procedure, it is still far from perfected. It was found that the usable range of pH is quite small and difficult to maintain. Excess TMAH, only a little beyond that needed to neutralize the SA, resulted in significant attack on the aluminum bonding pads. Insufficient TMAH, as evidenced by the failure of the mixture to become reasonably clear after 10 min of vigorous stirring at 80 °C, produced etching problems similar to those encountered with our interpretation of the procedure of [18], including poor reproducibility of the depth of the etch pit from pixel to pixel.

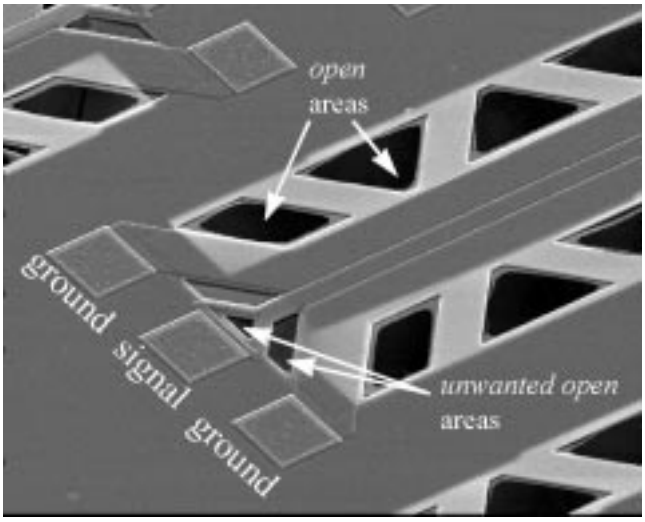


Fig. 7. Anisotropic postprocessing etching of microwave coplanar waveguide.

IV. Hybrid Technique

In general, transmission-line elements over silicon are very lossy at microwave frequencies, and unwanted silicon must be removed in order to electromagnetically decouple the transmission lines from the lossy silicon substrate. These transmission lines, used in telecommunications, are the high-frequency equivalent of dc coaxial lines. The hybrid micromachining technique presented here was motivated by our work on the development of microwave coplanar waveguides (transmission lines) and other passive microwave sensors and components [7]. This method is very general and can be applied to fabricate any large microstructure.

For commercial applications, these waveguides must meet two stringent requirements: good low-loss performance and mechanical robustness. The performance of these first-generation [see Fig. 7(c)] coplanar microwave transmission lines with 50-Ω nominal characteristic impedance meets the design goals of 2–4-dB/cm attenuation over the frequency range 1–40 GHz. Without micromachining the silicon underneath the waveguides, the observed loss of $\sim$35 dB/cm at 35 GHz was too high and rendered the waveguide impractical [7]. Thus, removing the lossy silicon is essential to obtaining good microwave-frequency performance. Since the waveguide is completely suspended, its mechanical robustness is an important issue.

The design of miniature microwave waveguides is realized by placing the glass openings in the appropriate locations around the waveguides to expose the underlying silicon for micromachining. In earlier experiments, attempts were made to fabricate 2–3-mm-long waveguides using only anisotropic etching. The design requirements to achieve the overlapping of etch pits to form one long etch pit beneath the waveguide were very strict and allowed very little variation in metal linewidths. An SEM micrograph of an early coplanar waveguide in CMOS is shown in Fig. 7. In the figure, a number of disadvantages are apparent. The supporting glass remains in relatively small areas due to the overlapping etch design requirements. This weakens the structure. Also, as pointed out in Fig. 7, in order to etch beneath the waveguide and connect all individual etch pits into one large pit, a dielectric *open* must be placed in the center of the waveguide, resulting in awkward and reflective pad connections. More importantly, the etching progressed along the length of the waveguides, which took many hours, and required different etching procedure for different waveguide lengths. Due to the very long time in EDP, chips accrued substantial damage to the bond pads and supporting passivation. The longer waveguides were usually broken during wet anisotropic etching even at very low stirring rates, and the yields were very low. Moreover, excessive care had to be taken during cleaning and handling of those chips that survived the wet etch.

Combining the isotropic and anisotropic etch into the post-fabrication processing has many advantages. The design requirements are much more flexible due to the inherent undercutting of the isotropic etch. This means that the placement of glass openings no longer dictates the layout, and the openings require significantly smaller areas, leaving more mechanical support and more area for devices. On the other hand, the desirable etch stop control and depth of etch pits of the anisotropic etch are also obtained, but with much less etch time required.

The hybrid micromachining method consists of a two-step process in which an isotropic etch undercuts the masks to remove all the silicon, and an anisotropic etch forms a well-controlled deep V-shape channel. Because the first step is isotropic etching to remove all the silicon beneath the waveguides, the glass openings should be placed in such a way that the etched regions formed by two adjacent openings on opposite sides of the waveguides merge together directly beneath the center of the device. A section of a completed waveguide before and after XeF_2 etching is shown in Fig. 8(a) and (b), respectively. Even though most of the lossy silicon was removed, the bottom is still close enough for the microwave fields to "see" the silicon substrate. The second step consists of an anisotropic etch in either EDP or TMAH to create a well-defined deep V-shape pit as shown in Fig. 8(c). As usual for anisotropic etchants, there is a tradeoff between process compatibility and reproducibility. Higher yields have

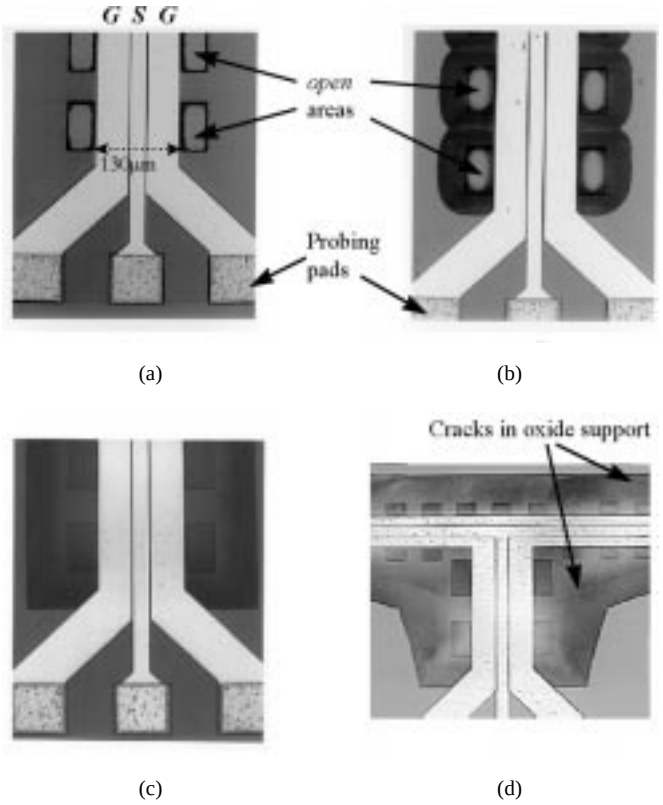


Fig. 8. Hybrid postprocessing etching. (a) Microwave coplanar waveguide as fabricated by a commercial foundry. (b) After XeF_2 etching. (c) After hybrid etching. (d) A section of the T-shaped waveguide.

been obtained using EDP than TMAH, but the finished chips etched in EDP tend to have long-term corrosion problems, which may possibly be eliminated by development of a better cleaning procedure.

The hybrid micromachining technique allows for fabrication of CMOS coplanar microwave devices by significantly reducing the etch time, yet preserves the anisotropic characteristics of the micromachining. This technique is very general and can be applied to make large microstructures of any size and length, including T-shaped structures such as the power divider T in Fig. 8(d). Fig. 9 is an example of a thermoelectric power sensor [22], which operates up to 20 GHz. We have used this etching technique to fabricate microwave power sensors, antennas, and microfluidic channels. Because this etching method is fully compatible with CMOS technology, it allows for on-chip integration of electronics for signal conditioning and communications. Future work will focus on using this hybrid micromachining technique to develop various CMOS-compatible microwave coplanar components and antennas for applications in telecommunications and well-defined long microfluidic channels for biochemical applications.

V. Conclusion

We have presented a novel postprocessing etching technique for fabricating large suspended microstructures in CMOS technology. Glass openings exposed the silicon for frontside etching and require no additional mask. The suspended

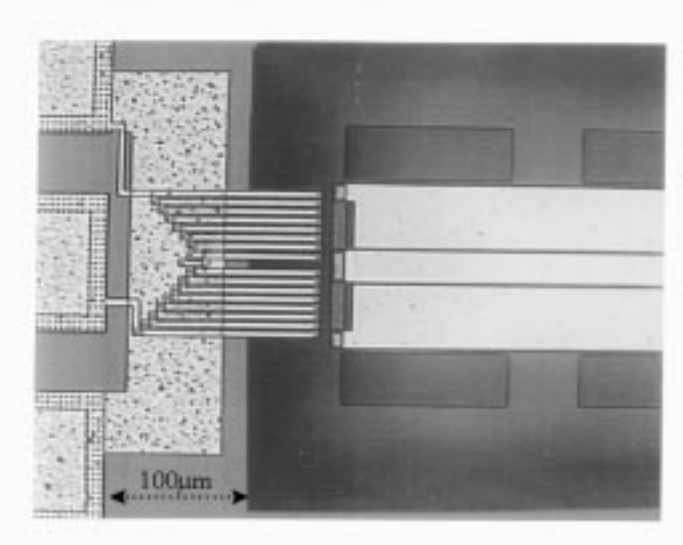


Fig. 9. Thermoelectric microwave power sensor fabricated in CMOS technology.

microstructures were realized by a combination of isotropic etching with gas-phase XeF_2 and anisotropic etching in either EDP or TMAH. The advantages and disadvantages of these etchants with respect to selectivity, reproducibility, and process compatibility were described in detail. An application of this technique to fabricate microwave coplanar transmission lines and thermoelectric power sensors was described. Implementation in CMOS technology allows the integration of electronics for signal processing and communications on the same chip as the suspended microstructures.

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